What we have learnt up to now?

- Basic semiconductor equations
- Drawing band diagrams for pn junctions, and npn/pnp transistors
- RTL/DTL/TTL/ATTL/STTL analysis
  - Analysis for states of each transistor
  - Transfer characteristics
  - Power dissipation
  - Definitions that relate to delay
  - Input/output currents, voltages
  - The problems/solutions of charge removal from base
- ECL basics
Announcements

Output impedance of Darlington pull-up circuit

Finish ECL
Announcements

- Exam on April 13th

- HW2 due this Friday (March 24th)

- Tutorial session on April 10 evening
Output impedance of Darlington pull-up circuit

The circuit is drawn as follows:

Assuming the output current is small the transistors $Q_P$ and $Q_{P2}$ will be active. Then, ignoring $R_{bb'}$, the equivalent model will be:
Output impedance of Darlington pull-up circuit

\[ r_{out} = \frac{\partial V_o}{\partial I_o} \]

\[ I_o = (\beta + 1)I_{B(QP2)} \]

\[ I_o = (\beta + 1) \left( (\beta + 1)I_{B(QP)} - \frac{V_o + 0.7}{R_{EP}} \right) \]

Ignoring the term with \( R_{EP} \)

\[ I_o = (\beta + 1)^2 \frac{V_{CC} - V_o - 2*V_{BEA}}{R_C} \]

\[ \frac{\partial V_o}{\partial I_o} = \frac{-R_C}{(\beta + 1)^2} \]
The basic circuit forming the basis of ECL gates is the "emitter coupled current switch".

The operation of the current switch is based on changing the transistor through which the current $I_{RE}$ flows. This change is fast, since the emitter current of an active npn transistor depends exponentially on the base-emitter voltage. For each 60mV change in the base-emitter bias, the emitter current of an active npn changes by $exp\left(\frac{V_{BE}}{kT}\right)$.
The basic circuit forming the basis of ECL gates is the "emitter coupled current switch".

\[ \text{Vin} < \text{Vref} \]
\[ \text{Vin} = \text{Vref} \]
\[ \text{Vin} > \text{Vref} \]
Assume $V_{IH} - V_{IL} = 100mV$

$V_{in} < V_{ref} - 0.05 :: Q_I$ is OFF, $Q_R$ is ACT

$V_{in} > V_{ref} + 0.05 :: Q_I$ is ACT, $Q_R$ is OFF

In order to guarantee ACT operation, the resistor, input voltage range, and power supply voltages must be selected APPROPRIATELY.

ECL standard ::

$V_{CC} = 0V, V_{EE} = -5.2V, V_{ref} = -1.175V$

So:

$V_{in} < V_{ref} - 0.05 :: V_{CQI} = V_{CC}$

$V_{in} > V_{ref} + 0.05 :: V_{CQI} = V_{CC} - R_{CC}I_{RE}$
ECL gates

“emitter coupled current switch”

Basic ECL gate
ECL gates

The emitter followers (Q_INV \(- R_o \) and Q_NINV \(- R_o \)) provide extremely low output impedance. Thereby increasing the capacity to feed high number of fan-out gates.
ECL gates

Output impedance of emitter follower

Emitter follower and model

The output resistance consists of $R_{bb'}$ as seen from the output in parallel with $R_o$. 
ECL gates

Output impedance of emitter follower

Model of emitter follower

Derivation HERE
Consider node NINV with $V_{IN} = \text{logic0}$

$V_{IN} < V_{ref} - 0.05$ (LOW voltage)

Now: $Q_I$:: OFF, $Q_R$::ACT

$I_{RE} = \frac{V_{ref} - V_{BEA} - (-V_{EE})}{R_E}$

$I_{RCR} = \alpha I_{RE}$

$I_{RCR} = \alpha \frac{V_{ref} - V_{BEA} - (-V_{EE})}{R_E}$

$V_{BQ_{NINV}} = 0 - R_{CR} \times I_{RCR}$

The node (NINV) is now at logic 0 value, which is:

$V_{OL} = V_{BQ_{NINV}} - V_{BEA} = 0 - R_{CR} \times I_{RCR} - V_{BEA}$

$V_{OL} = V_{BQ_{NINV}} - V_{BEA} = 0 - R_{CR} \times \alpha \frac{V_{ref} - V_{BEA} - (-V_{EE})}{R_E} - V_{BEA}$

The resistor values and $V_{EE}$ is selected so that $V_{OL} \approx -2 \times V_{BEA}$

Assume $V_{IH} - V_{IL} = 100\,\text{mV}$

ECL inverter transfer characteristic: NINV
ECL inverter transfer characteristic: NINV

Use $V_{BEA} = 0.75\text{V}$ for ECL

NINV with $V_{IN}=\text{logic0 (LOW)}$

\[
V_{OL} = -R_{CR} \times \alpha \left( \frac{V_{ref} - V_{BEA} - (-V_{EE})}{R_E} \right) - V_{BEA}
\]

\[
V_{OL} = -300 \times 0.98 \times \frac{-1.175 - 0.75 - (-5.2)}{1240} - 0.75 = -1.526\text{V}
\]

Note that this is for NINV output.
ECL inverter transfer characteristic: NINV

Use $V_{BEA} = 0.75V$ for ECL

NINV with $V_{IN} = \text{logic1 (HIGH)}$

$V_{IN} > V_{ref} + 0.05$ (LOW voltage)

Then, node NINV will be at logic1 (HIGH)

$V_{OH} = 0 - V_{BEA} = -0.75V$

Note that this is for NINV output.
Use $V_{BEA} = 0.75V$ for ECL

For $(V_{ref} - 0.05) < V_{IN} < (V_{ref} + 0.05)$ the logic state is indeterminate. $Q_I$ is switching from OFF to ACT. $Q_R$ is switching from ACT to OFF.

Assume $\overline{V_o}$ (NINV) changes linearly as $V_{IN}$ changes from $V_{ref} - 0.05$ to $V_{ref} + 0.05$. 
ECL inverter transfer characteristic: \textbf{NINV}

![ECL characteristics graph]

- Non-inverting output

Vin

Outputs

-1.6
-1.5
-1.4
-1.3
-1.2
-1.1
-1.0
-0.9
-0.8
-0.7
-0.8
-0.9
-1.0
-1.1
-1.2
-1.3
-1.4
-1.5
-1.6

Vin

Non-inverting output
ECL inverter transfer characteristic: INV

NINV with $V_{IN} = \text{logic0 (LOW)}$

$V_{IN} < V_{ref} - 0.05$ (LOW voltage)

Now: $Q_I:: \text{OFF}, Q_R::\text{ACT}$

Node INV ($V_{out}$) is at logic1 (HIGH)

$V_{OH} = V_{CC} - V_{BEA} = -0.75V$

Note that this is for INV output.

For

$(V_{ref} - 0.05) < V_{IN} < (V_{ref} + 0.05)$

the logic state is indeterminate.

$Q_I$ is switching from OFF to ACT.

$Q_R$ is switching from ACT to OFF.

When $V_{IN} > (V_{ref} + 0.05)$ $Q_I$ is ACT.

Assume $V_o$ (INV) changes linearly as $V_{IN}$ changes from $V_{ref} - 0.05$ to $V_{ref} + 0.05$. 
ECL inverter characteristic: NINV & INV

ECL characteristics

 Vin
-1.6 -1.5 -1.4 -1.3 -1.2 -1.1 -1.0 -0.9 -0.8 -0.7

outputs
-1.6 -1.5 -1.4 -1.3 -1.2 -1.1 -1.0 -0.9 -0.8 -0.7

NON–inverting output

inverting output
Consider node INV with $V_{IN}=\text{logic1}$

$V_{IN} > V_{ref} + 0.05$ (HIGH)

Now: $Q_I:: \text{ACT}, Q_R:: \text{OFF}$

$I_{RE} = \frac{V_{IN} - V_{BEA} - (-V_{EE})}{R_E}$

$I_{RCI} = \alpha I_{RE}$

$I_{RCI} = \alpha \frac{V_{IN} - V_{BEA} - (-V_{EE})}{R_E}$

$V_{BQ_{NINV}} = 0 - R_{CI} * I_{RCI}$

The node (INV) is now at logic 0 value, which is:

$V_{OL(INV)} = V_{BQ_{NINV}} - V_{BEA} = 0 - R_{CI} * I_{RCI} - V_{BEA}$

$V_{OL(INV)} = 0 - R_{CI} * \alpha \frac{V_{IN} - V_{BEA} - (-V_{EE})}{R_E} - V_{BEA}$
ECL inverter transfer characteristic: INV

The resistor value $R_{CI}$ selected to be smaller than $R_{CR}$ so that $V_o = V_{OL}$ for $V_{IN} = V_{OH}$

Use $V_{BEA} = 0.75V$ for ECL

INV with $V_{IN} > (V_{ref} + 0.05) = \text{logic1}(\text{HIGH})$

$$V_{OL} = 0 - R_{CI} * \alpha \frac{V_{IN} - V_{BEA} - (-V_{EE})}{R_E} - V_{BEA}$$

$$V_{OL} = -270 \times 0.98 \times \frac{V_{IN} - 0.75 - (-5.2)}{1240} - 0.75$$

$$V_{OL} = -0.213 \times V_{IN} - 1.7$$

Note that this is for NINV output.
### ECL inverter characteristic: NINV & INV

<table>
<thead>
<tr>
<th>Vin</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1.6</td>
<td>-1.5</td>
</tr>
<tr>
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<td>-1.4</td>
</tr>
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</tr>
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<td>-0.8</td>
<td>-0.7</td>
</tr>
</tbody>
</table>

![ECL characteristics](image-url)
As $V_{IN}$ increases further, $Q_I$ will saturate when $V_{CE(Q_I)} = V_{CES}$

Assume $V_{BCS} = 0.7V$
Assume $V_{CES} = 0.05V$

$$V_{C(Q_I)} = 0 - R_{CI} \cdot \alpha \frac{V_{IN} - V_{BEA} - (-V_{EE})}{R_E}$$

$$V_{E(Q_I)} = V_{IN} - V_{BEA}$$

Rather than try to remember Eq. 6.23, just use

$V_{CE(Q_I)} = V_{CES}$ for condition of saturation. When saturation of $Q_I$ happens

$$V_o = V_{IN} + V_{BCS} - V_{BEA}$$
ECL inverter transfer characteristic: INV

As $V_{IN}$ increases further, $Q_I$ will saturate when $V_{CE(Q_I)} = V_{CES}$

Assume $V_{BCS} = 0.7V$
Assume $V_{CES} = 0.05V$

$$V_{C(Q_I)} = -270 \times 0.98 \frac{V_{IN} + 4.45}{1240} = -0.213 \times V_{IN} - 0.95$$

$$V_{E(Q_I)} = V_{IN} - 0.75$$

Solving for $V_{CE(Q_I)} = 0.05$

$V_{IN_{sat}} = -0.21V$
ECL inverter characteristic: NINV & INV
ECL inverter characteristic: NINV & INV

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>LOGIC</th>
<th>$V_o$ (INV)</th>
<th>$\overline{V_o}$ (NINV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN} &lt; -1.180$</td>
<td>LOGIC0</td>
<td>-0.75</td>
<td>-1.523</td>
</tr>
<tr>
<td>$V_{IN} &gt; -1.170$</td>
<td>LOGIC1</td>
<td>LOW</td>
<td>-0.75</td>
</tr>
<tr>
<td>$V_{IN} &gt; -0.21$</td>
<td>INVALID</td>
<td>SAT</td>
<td>-0.75</td>
</tr>
</tbody>
</table>
ECL inverter characteristic: Motorola-SPECs

Typical and AVERAGE characteristics
ECL inverter characteristic: Motorola-SPECs

\[ NML = |V_{OL(max)} - V_{IL(max)}| = |-1.5 + 1.325| = 0.175 V \]

\[ NMH = |V_{OH(min)} - V_{IH(min)}| = |-0.85 + 1.025| = 0.175 V \]

(note that the definitions are somewhat different than the ones used in the book)
ECL inverter power dissipation

ECL power dissipation dominated by DC dissipation. This is an approximation and will not hold at higher frequencies. Still, we will only consider DC dissipation of ECL gates. 

\( P_L \) is the DC dissipation when NONINVERTING output is LOW. 

\( P_H \) is the DC dissipation when NONINVERTING output is HIGH.

\[
\begin{align*}
P_L &= -(-V_{EE}) \cdot I_{EE} = V_{EE} \cdot I_{EE} = V_{EE} \cdot (I_{RE} + I_1 + I_2)
\end{align*}
\]
ECL inverter power dissipation

\[ P_L = -(V_{EE}) \times I_{EE} = V_{EE} \times I_{EE} = V_{EE} \times (I_{RE} + I_1 + I_2) \]

\[ I_{RE} = \frac{V_{ref} - V_{BEA} + V_{EE}}{R_E} \]

\[ I_1 = \frac{V_{OH} + V_{EE}}{R_E} \]

\[ I_2 = \frac{V_{OL} + V_{EE}}{R_E} \]
ECL inverter power dissipation

\[ P_H = -(-V_{EE}) * I_{EE} = V_{EE} * I_{EE} = V_{EE} * (I_{RE} + I_1 + I_2) \]

\[ I_{RE} = \frac{V_{OH} - V_{BEA} + V_{EE}}{R_E} \]

\[ I_1 = \frac{V_{OL} + V_{EE}}{R_E} \]

\[ I_2 = \frac{V_{OH} + V_{EE}}{R_E} \]
ECL inverter power dissipation

\[ P_{DC} = \frac{P_L + P_H}{2} \]
This specific circuits power dissipation to be asked in next quiz.
Using OR-NOR and inverter-buffer gates is much easier in ECL. Also:
If we connect output of 2 ECL gates, the outputs are logically "OR"ed.

The reason why OR-NOR is to be preferred will be asked in next quiz. ECL implementation of a given logic function to be asked in the next quiz.
ECL temperature dependence

The main source of temperature dependence comes from $V_{BEA}$ and $V_D$.

$$\frac{\partial V_{BE}}{\partial T} \approx -2mV/°C$$

$V_D$ (diode built-in potential) also shows a similar change.
ECL temperature dependence

Considering the basic ECL inverter/buffer:
Output high level is given as:

\[ V_{OH} = -V_{BEA} \]

So:
\[ \frac{\partial V_{OH}}{\partial T} = 2 \text{mV/}^\circ \text{C} \]

Output low level is given as:

\[ V_{OL} = -R_{CI} \alpha \frac{V_{IN} - V_{BEA} - (-V_{EE})}{R_E} - V_{BEA} \]

So:
\[ \frac{\partial V_{OL}}{\partial T} = - \frac{R_{CI}}{R_E} \left( \frac{\partial V_{OH}}{T} - \frac{V_{BEA}}{T} \right) - \frac{V_{BEA}}{T} \approx 1 \text{mV/}^\circ \text{C} \]
ECL temperature dependence

With increasing temperature, the NMH decreases and NML increases. The overall effect is a decrease in the noise margin. It would be better to "compensate" so that the NM decreases slower.
ECL family: ECL I

Decouples grounds for switch and emitter followers.
ECL family: ECL I/III/10k

Has temperature compensated reference.
ECL family: ECL I/III/10k, temperature compensation

$\delta$ represents the change in junction voltage.
ECL family: ECL I/III/10k, temperature compensation

\[ \Delta V_R = \frac{2\delta R_1}{R_1 + R_2} - \delta \approx -0.77\delta \]

\[ \Delta V_{outLOW} = -\Delta V_R \frac{R_C}{R_E} + \delta \frac{R_C}{R_E} - \text{delta} \]

\[ \Delta V_{outHIGH} = -\delta \]

\[ \Delta V_{out}(\text{AVERAGE}) = \frac{\Delta V_{outLOW} + \Delta V_{outHIGH}}{2} \approx -0.77\delta \]

Since average change in output levels is equal to change in \( V_R \), \( V_R \) stays at midpoint of logic transition range. Hence, the NML and NMH changes equally. But NML and NMH still does change.
ECL family: ECL 100k

Has constant current source (reducing dependence on $V_{EE}$)
Diodes and R reduce temperature coefficients of $V_{OL}$ and $V_{OH}$.
Also has better temperature compensatesed reference voltage supply.
ECL family: Level sensitive active pull-down

Definitely makes a nice HW-quix/exam question.

Active pulldown decreases $L_{tLH}$.

$V_{REG} = V_{OL} - V_{BEA}$. 
Omission Note:

Not responsible from sections 6.10.1 and 6.11
Next Lecture Hour:

Will finish ECL.
Finish reading ECL in preparation of quiz.
Will start MOS.
Make a quick reading of MOS chapter for quiz.