Today's Goals

- Finish MOS transistor
- Finish NMOS logic
- Start CMOS logic
MOS Capacitor Equations

- **Threshold voltage**
- **Gate capacitance**

\[ V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{II}}{C_i} - \frac{Q_d}{C_i} + 2\Phi_F \]

**Contributions to threshold voltage**

For enhancement type devices:
for n-channel devices threshold voltage > 0
p-channel devices threshold voltage < 0

\[ C_i = \epsilon_0 \frac{\epsilon_{ox}}{t_{ox}} WL \]
MOS Capacitor Characteristics

- You MUST know/understand MOS capacitor threshold voltage formula
- You MUST know/understand/be able to draw MOS capacitor band diagrams

Refer to Streetman's book for details !!
MOS Transistor Operation

- $I_G = 0$
- $I_D = 0$ when $V_{GS} < V_T$
- $I_D$ saturates when $V_{GD} < V_T$

Pinch-off is an “educational tool” to justify saturation. At the drain end the electrons are out-of equilibrium, so the equilibrium concentration formula does NOT apply.

Pinch-off occurs due to velocity saturation at drain end of the channel.
FIGURE 2.5. nMOS device behavior under the influence of different terminal voltages.
MOS Transistor I-V characteristics

- Analytical derivation assumes “Long channel”
- “Long channel” implies uniform electric field within the channel
- Do you think measured values will match the analytical formula? Even for a physically long device?
- What can be done to predict the I-V curve of a transistor before fabrication?
- You are not responsible from the derivation of the transistor IV.
- You must be able to draw and understand the transistor band diagram.
MOS Transistor I-V characteristics

- Operation Regimes:
  - Off
  - Linear
  - Saturated

- Can you write equations for both NMOS and PMOS?

Device transconductance parameter:

\[ K = \frac{W}{L} \frac{\mu \varepsilon_{ox}}{t_{ox}} \]

Process transconductance parameter:

\[ \dot{k} = \frac{\mu \varepsilon_{ox}}{t_{ox}} \]

\[ I_G = 0 \]
MOS Transistor I-V characteristics

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  - Off
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Device transconductance parameter:

\[ K = \frac{W \mu \varepsilon_{ox}}{L \ t_{ox}} \]

Process transconductance parameter:

\[ \dot{k} = \frac{\mu \varepsilon_{ox}}{t_{ox}} \]
**MOS Transistor I-V characteristics**

**NMOS**

\[ V_T > 0 \]

\[ V_{GS} < V_T \Rightarrow \text{OFF} \]

\[ V_{GS} > V_T \land V_{DS} < V_{GS} - V_T \Rightarrow \text{LINEAR} \]

\[ V_{GS} > V_T \land V_{DS} > V_{GS} - V_T \Rightarrow \text{SAT} \]

\[ I_{DS} > 0 \]

When linear

\[ I_{DS} = K_N \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

When SAT

\[ I_{DS} = \frac{K_N}{2} (V_{GS} - V_T)^2 \]
MOS Transistor I-V characteristics

- **PMOS**

  \( V_T < 0 \)

  \( V_{GS} > V_T \Rightarrow \text{OFF} \)

  \( V_{GS} < V_T \land \ V_{DS} > V_{GS} - V_T \Rightarrow \text{LINEAR} \)

  \( V_{GS} < V_T \land \ V_{DS} < V_{GS} - V_T \Rightarrow \text{SAT} \)

  \( I_{DS} < 0 \)

  When linear

  \[
  I_{DS} = -K_P \left[ \left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2} \right]
  \]

  When SAT

  \[
  I_{DS} = -\frac{K_P}{2} (V_{GS} - V_T)^2
  \]
MOS Transistor I-V characteristics

- **NMOS/PMOS**

\[
\begin{align*}
V_{GS} &< V_T \Rightarrow \text{OFF} \\
V_{GS} &> V_T \land V_{DS} < |V_{GS} - V_T| \Rightarrow \text{LINEAR} \\
V_{GS} &> V_T \land V_{DS} > |V_{GS} - V_T| \Rightarrow \text{SAT}
\end{align*}
\]

When linear

\[
|I_{DS}| = K \left[ \left( V_{GS} - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right]
\]

When SAT

\[
|I_{DS}| = \frac{K}{2} \left( V_{GS} - V_T \right)^2
\]
MOS Transistor I-V characteristics

- You MUST memorize NMOS/PMOS transistor I-V equations and characteristics
MOS Secondary effects

- Body effect
- Subthreshold current
- Transit time
- Short channel effect
- Channel length modulation
- Velocity Saturation
- Gate leakage

In fact, extremely important for MODERN MOS LOGIC.

But complicates a first study of MOS LOGIC.

These will be studied later, when we need them.
NMOS Logic

- 3 types of pull-up devices
- Has static power dissipation
- Low-to-High delay is large
- Was used when there was no p-type MOS around
Resistor load NMOS Logic VTC

- $I_{LOAD} = 0$

- Identify the mode of the transistor and solve for $I_R = I_{DS(MN)}$

- **OBSERVE:** correct logic depends on the values of $R$ and $K$
Resistor load NMOS Logic VTC

\[ V_I < V_T \Rightarrow M_{NO} \text{ OFF} \]
\[ I_{DMNO} = 0 \]
\[ V_O = V_{DD} \]

\[ V_i = V_{DD} \Rightarrow M_{NO} \text{ LINEAR} \]
\[ I_D = K \left( (V_{DD} - V_T) V_O - \frac{V_O^2}{2} \right) \]
\[ I_R = \frac{V_{DD} - V_O}{R} \]

Solve for \( V_O \) from \( I_D = I_R \)

Ignore the \( V_o^2 \) term to get

\[ V_O = \frac{V_{DD}}{R K (V_{DD} - V_T) + 1} \]
Resistor load NMOS Logic VTC

Is $M_{NO}$ really in LINEAR region?

\[ K \approx 1 \frac{mA}{V^2} \]

Assume $R \approx 100$ Ohm

Assume $V_T = 1V$

\[ V_O = \frac{5}{100 \times 0.0014 + 1} = 3.5V \]

\[ V_{DS} = 3.3 < 5 - 1 \]

Yes device is linear

BUT $V_O > V_T$.

If $R = 1000$ Ohm

\[ V_O \approx 0.1V < V_T \]

Correct logic operation depends on $R$ and $K$
Depletion load NMOS Logic VTC

- \( I_{LOAD} = 0 \)
- Identify the mode of the transistor and solve for \( I_{DS(ML)} = I_{DS(MN)} \)
- OBSERVE: correct logic depends on the values of \( K_L \) and \( K_O \)
NMOS Power dissipation

- $P_H = 0$
- $P_L = V_{DD} \times I_{DDL}$
- Dynamic power dissipation important

$$P_{AC} = f C_L V_{DD}^2$$
NMOS Delay

- Time to change output half-way
- Assume current stays equal to initial value after switching
Digital Device Definitions
- Physical Basics
- Diodes
- BJTs
- RTL-DTL-TTL
- ECL
- MOS transistors
  - MOS capacitors
  - MOS transistor I-V
  - MOS secondary effects
- NMOS logic
  - Transfer characteristics
  - Power dissipation
  - Delay
  - Fan-out
- Logic design
- CMOS logic
  - Transfer characteristics
  - Power dissipation
  - Delay
  - Fan-out
- Logic design
- Layout
- BiCMOS logic
  - Transfer characteristics
  - Power dissipation
  - Delay
  - Fan-out
- Interfacing
- Bistable circuits

NMOS Fan-Out

- Fan out limited by tpmax imposed by system design
NMOS logic design

- Design the pull-down network
- Select the Kp of pull-up transistor
- Pull-down network:
  - Write down your logic function as \( f_0 = \text{NOT}(f_{pd}) \)
  - The AND blocks in \( f_{pd} \) will appear in series
  - The OR block in \( f_{pd} \) will appear in parallel
  - Minimization of \( f_{pd} \) for reduction in transistor count necessary