Design a CMOS circuit that will multiply two 4 bit binary (unsigned) integers. For simplifying the process, we are asking the design be based on a decremener and an adder/accumulator. This is not the way in which a multiplier would be implemented, but the suggested design works well to demonstrate the basic issues in CMOS gate optimization and CMOS layout. Furthermore, the suggested design is the simplest approach amongst the many possible. The simplicity is achieved at the expense of multiplication time.

You are required to use the tools that we are distributing on the CD. All of the programs there are GPLvled, so there are no license issues.

The design cycle will be as follows:

1. Make a gate level design in verilog. Simulate for functionality, and try to optimize for delay.
2. Implement the gate level design in SPICE. Simulate to demonstrate functionality and estimate delay. If necessary, optimize gate level design by going back to step 1.
3. Make the layout. Extract spice netlist and simulate to obtain a better estimate for delay. Go back to step 1 for further optimization if necessary.

You will need to learn a lot on your own, but if you feel stuck please do not hesitate to ask me or any one of the TAs.