Fraunhofer
IIS

Offer for a 3-Months Internship for Bachelor or Master Students

The offer is for bachelor or master students with the option to continue for a final thesis

Topic:
Programming of Circuit Generators for an Intelligent Analog IP Library (IC Design Flow Development)

Supervisor: Uwe Eichler
Design Automation Division EAS in Dresden

Abstract:
With growing challenges for current CMOS processes with feature sizes of less than 100nm, analog circuit components gain more importance. In contrast to digital, analog design is still very rarely automated and thus inefficient and cost-intensive. We develop innovative design methods for integrated analog circuits together with manufacturers and EDA companies. By means of a new design methodology, based on an intelligent IP library, the analog design flow is to be highly automated and made more efficient. Actual demands of ASIC suppliers like technology migration, parametrization, "Design for Manufacturing", "Design for Reliability" will find special consideration in this library.

Tasks:
The task is primarily addressed to students, who are interested in software development within a novel design flow for microelectronic circuits (e.g. for automotive, bio-medical, and industrial applications). Beyond that, useful skills in the field of integrated circuit design and corresponding design methodologies can be obtained.

- programming of parametrizable circuit and layout generator scripts for available basic circuits
- implementation of techniques to improve design reliability (e.g. prevention of
- electromigration or latch-up effects)
- preparation of circuit and test bench generators for circuit optimization tools

The tasks can be carried out in the context of an internship and/or a final thesis and will be defined individually according to your experiences and interests. You will be assisted in technical and organizational questions and work in close cooperation with the project team.

Requirements:

- pleasure in programming
- basic knowledge of analog circuits is beneficial
- experiences with analog design tools from Cadence are beneficial

Fraunhofer
IIS

Payment Conditions & Application:
Fraunhofer IIS will pay an appropriate allowance to cover living costs and will also provide for accommodation and medical insurance during your stay in Dresden. Travel expenses will not be reimbursed.

If you are interested in the afore-mentioned topic please send your formal application including CV, a copy of your *valid* passport or ID card, motivation letter, latest grades report and the date of your earliest possible start to:

Nail Akar, PhD
Student Exchange Coordinator
EEE Department
Bilkent University
akar@ee.bilkent.edu.tr
Tel: ++90-312-290 2337
Fax: ++90-312-266 4192

About the Institute's Division Design Automation – EAS in Dresden:
The design of circuits and systems is bridging first specifications to engineering data for manufacturing and, therefore, it is considered to be an important part of the value creation chain from the first idea to the market launch of products. The models, methods, and tools developed and provided by us are designed for an efficient design process from product specifications into integrated circuits, boards, devices, or components. They complement commercial tools, improve application specific design flows, include specifics in process of implementation, and enable designers to increase their efficiency and the quality of designs.

For further information please visit our website: www.eas.iis.fraunhofer.de